REMARKS

The present application was filed on July 22, 2003 with claims 1-21. In the outstanding Office Action dated August 17, 2005, the Examiner has: (i) objected to the drawings; (ii) objected to the specification; (iii) rejected claims 1-21 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. US 2004/0001427 to Belotserkovsky et al. (hereinafter "Belotserkovsky"), in view of one or more of U.S. Patent No. 5,940,450 to Koslov et al. (hereinafter "Koslov") and U.S. Patent Publication No. US 2003/0231718 to Jiang (hereinafter "Jiang").

In this response, the specification has been amended in a manner which is believed to address the Examiner's objection. Additionally, Applicant traverses the §103(a) rejections. Applicant respectfully requests reconsideration of the present application in view of the above amendments and the following remarks.

The drawings have been objected to under 37 C.F.R. §1.83(a) for failing to show every feature of the invention specified in the claims. Specifically, the Examiner contends that "the Viterbi decoder recited in claim 10 must be shown or the feature(s) canceled from the claim(s)" (Office Action; page 2, paragraph 2). Applicant respectfully disagrees with this contention.

As set forth in 35 U.S.C. §113, a drawing need only be furnished "where necessary for the understanding of the subject matter sought to be patented." Applicant submits that the Viterbi decoder recited in claim 10 is not essential for a proper understanding of the invention, but rather a Viterbi decoder is merely one type of decoding scheme which can be used by the orthogonal frequency division multiplexing receiver, as is generically set forth in claim 1 and illustrated, for example, in FIG. 1. The present specification makes it clear that such a Viterbi decoder is within the scope of the claimed invention, stating that receiver 106 depicted in FIG. 1 may also include a Viterbi decoder "connected between the FDQ 132 and the slicer 134, assuming a trellis encoder is employed in the transmitter 102" (specification; page 10, lines 1-3). Consequently, Applicants do not believe that such additional limitation of claim 10 needs to be explicitly depicted in the drawings. Nevertheless, Applicants submit that the additional Viterbi decoder feature recited in claim 10 is shown generally in FIG. 1 as part of the connection arrangement between FDQ 132 and Slicer 134 in receiver 106.

For at least the above reasons, Applicant asserts that all elements recited in the claims that are necessary for a proper understanding of the invention are clearly depicted in the drawings. Accordingly, withdrawal of the objections to the drawings is respectfully solicited.

Claims 1-6, 8-16 and 18-21 stand rejected under §103(a) as being unpatentable over Belotserkovsky in view of Koslov. With regard to independent claims 1, 13 and 21, which are of similar scope, the Examiner contends that Belotserkovsky discloses all of the elements set forth in the subject claims, but acknowledges that "Belotserkovsky et al. does not teach a CFO estimation circuit" (Office Action; page 4, paragraph 3). However, the Examiner further contends that "Koslov et al. discloses a frequency error detection circuit . . . carrier recovery method that estimates frequency error by determining the difference in phase errors between two symbols" (Office Action; page 4, last paragraph). Applicant respectfully disagrees with the Examiner's contentions.

Claims 1, 13 and 21 are clearly distinguishable from the prior art of record, when considered either individually or in combination. Specifically, not only does Belotserkovsky fail to disclose a CFO estimation circuit, as acknowledged by the Examiner, but Belotserkovsky also fails to teach or suggest a CFO compensation circuit "configurable for receiving the baseband signal and modifying a phase of the baseband signal in response to a first control signal," as recited in claim 1. The Examiner contends that the CFO compensation circuit set forth in claim 1 is analogous to the carrier frequency adjustment module 64 shown in FIG. 3 of Belotserkovsky, "wherein adjusting the frequency inherently/implicitly changes the phase of the input signal" (Office Action; page 4, paragraph 3). Applicant respectfully disagrees with this contention. As is well known in the art, phase describes where in its cycle a periodic waveform is at any given point in time, while frequency describes the number of repetitions per unit of time of a complete waveform (*The American Heritage Dictionary of the English Language*, Fourth Edition, Houghton Mifflin Company, 2000). The phase of two waveforms having different frequencies may be the same (e.g., as in the case of harmonics). Thus, adjusting the frequency of a waveform does not necessarily directly translate to adjusting the phase of the waveform (and vice versa) as the Examiner suggests.

As stated in Applicant's prior response dated November 29, 2004, the carrier frequency adjustment module 64 taught by Belotserkovsky fails to disclose any mechanism for modifying a phase of the baseband signal, as required by claim 1, and is thus not analogous to the CFO

compensation circuit set forth in claim 1. Instead, Belotserkovsky states that the function of the carrier frequency adjustment module 64 is to introduce interbin interference into the input signal by changing the frequency offset (Belotserkovsky; page 2, paragraph [0026]). Consequently, the carrier frequency adjustment module taught by Belotserkovsky cannot reasonably be analogized to the CFO compensation circuit recited in claim 1. Moreover, the prior art of record fails to supplement the deficiencies of Belotserkovsky in at least this regard, and therefore the combination of Belotserkovsky and Koslov also fails to disclose the claimed invention.

Claim 1 is further distinguishable from the prior art of record in that the prior art fails to teach or suggest a CFO estimation circuit configurable for measuring a difference in phase error between at least two symbols received from the equalizer and for generating the first control signal which is representative of the phase error difference, as required by claim 1. The Examiner contends that Koslov, in FIG. 3, discloses a frequency error detection (FED) circuit (302) which "estimates frequency error by determining the difference in phase errors between two symbols (Office Action; page 4, last paragraph). Applicant respectfully disagrees with this contention.

The Examiner analogizes the FED circuit (302) taught by Koslov with the CFO estimation circuit recited in claims 1, 13 and 21. The FED circuit of Koslov "receives as its inputs the estimated phase error signal output by the phase detector 104 and the mode select signal generated by the mode select control circuit 118 and the sliced symbols" (Koslov; column 6, lines 24-27; emphasis added). As disclosed in Koslov, the FED circuit requires a phase error signal, which is "an imaginary part of the complex product of the equalized de-rotated symbol and the conjugate (Z_{sl}^*) of the sliced value (Z_{sl})" (Koslov; column 3, lines 40-42), as well as the sliced symbols as inputs, neither of which are utilized by the CFO estimation circuit recited in claim 1. In contrast to Koslov, however, the CFO estimation circuit of the claimed invention receives, as its only input, the baseband signal (prior to slicing) and generates the control signal which represents an estimation of the CFO present in the received signal. The recited prior art combination fails to teach or suggest this circuit configuration.

Furthermore, Koslov fails to explicitly teach or suggest using a CFO estimation circuit connected between the output of the equalizer and CFO compensation circuit in a feedback arrangement for modifying the phase of the baseband signal in response to a measured phase error

difference, as required by claim 1. Instead, Koslov, with reference to FIGS. 3 and 4, discloses the FED circuit 302 connected between a slicer module 106, a phase detector 104 and a second order filter 310 to form multiple feedback paths, neither of which are analogous to the claimed invention. The prior art of record thus fails to supplement the deficiencies of Belotserkovsky in at least this regard, and therefore the recited combination fails to disclose the invention set forth in the subject claims.

For at least the reasons set forth above, Applicant submits that independent claims 1, 13 and 21 are patentable over the prior art of record. Accordingly, favorable reconsideration and allowance of claims 1, 13 and 21 are respectfully requested.

With regard to claims 2-6 and 8-12, which depend from claim 1, and claims 14-16 and 18-20, which depend from claim 13, Applicant submits that these claims are also patentable over the prior art at least by virtue of their dependency from their respective base claims. Moreover, one or more of these claims define additional patentable subject matter in their own right. Accordingly, favorable reconsideration and allowance of claims 2-6, 8-12, 14-16 and 18-20 are respectfully requested.

Claims 7 and 17 stand rejected under §103(a) as being unpatentable over Belotserkovsky, in view of Koslov, and further in view of Jiang. While disagreeing with the Examiner's contention that Koslov and Jiang supplement the deficiencies of Belotserkovsky, Applicant asserts that claim 7, which depends from claim 1, and claim 17, which depends from claim 13, are also patentable over the prior art at least by virtue of their dependency from their respective base claims. Accordingly, favorable reconsideration and allowance of claims 7 and 17 are respectfully solicited.

In view of the foregoing, Applicant believes that claims 1-21 are in condition for allowance, and respectfully requests withdrawal of the §103 rejections.

Respectfully submitted,

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